Fig. 12

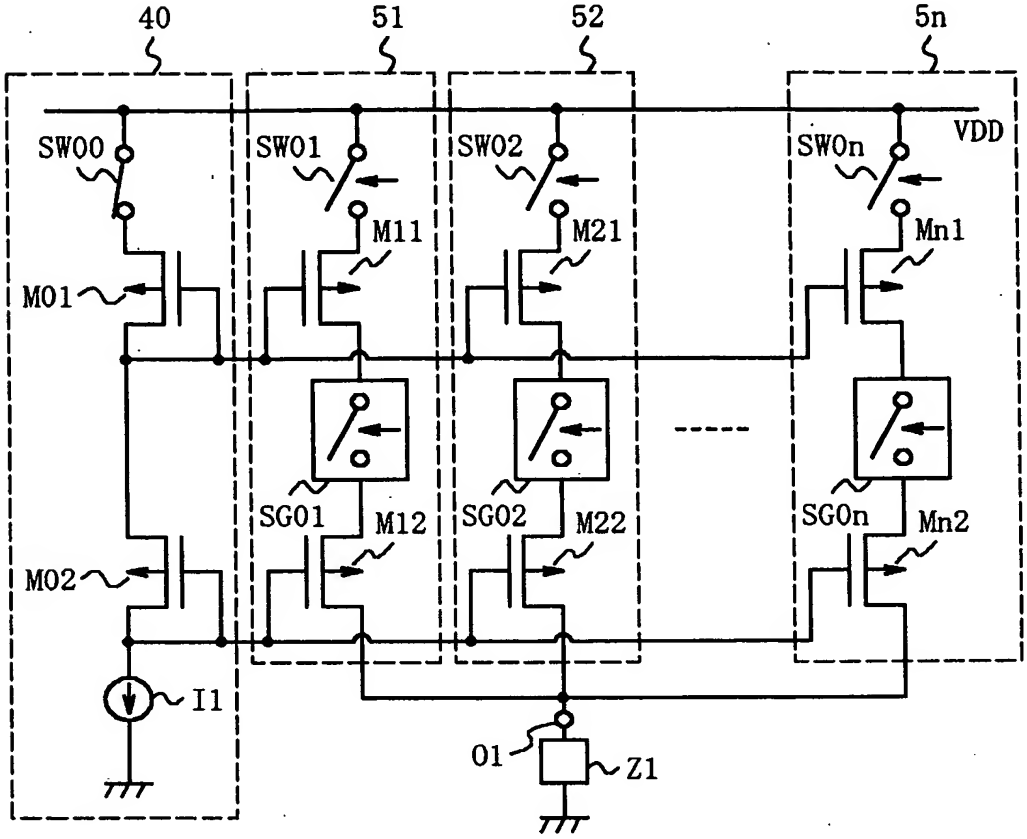


Fig. 1 (Prior Art)

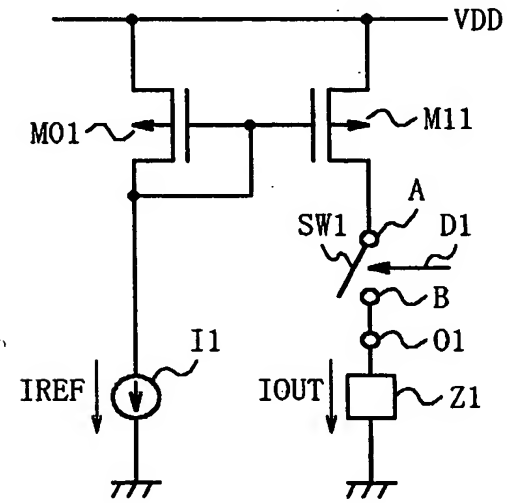


Fig. 2 (Prior Art)

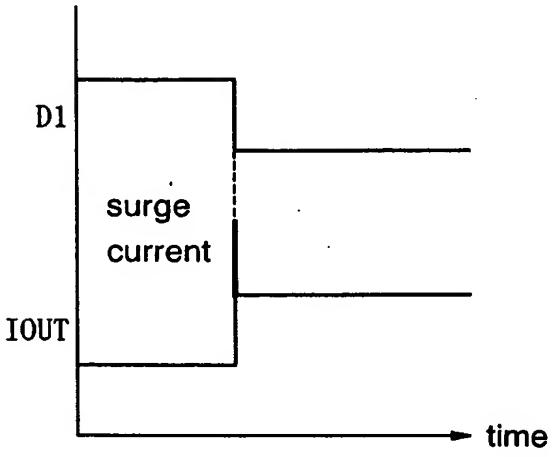


Fig. 3

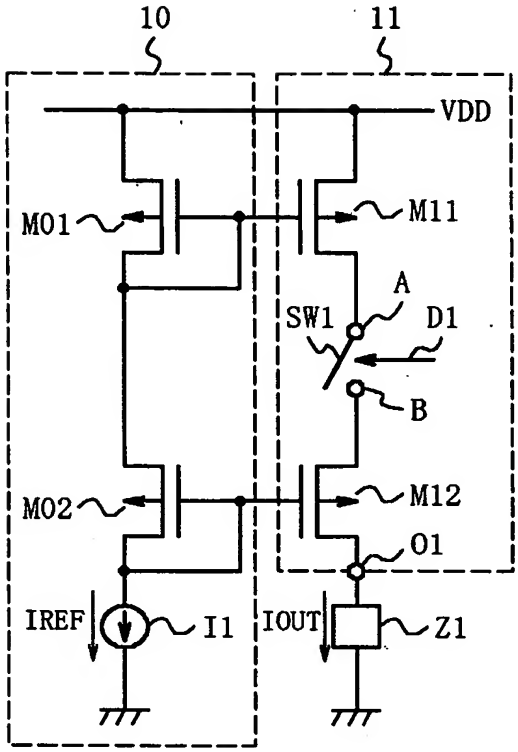

10
11
VDD
M01
M11
A
SW1
D1
B
M02
M12
O1
IREF
I1
IOUT
Z1

Fig. 4

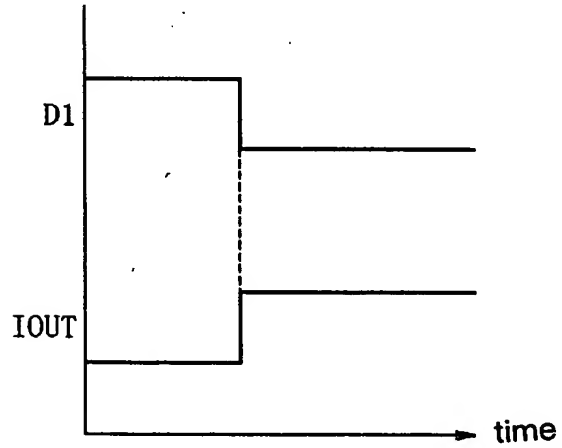

D1
IOUT
time

Fig. 5

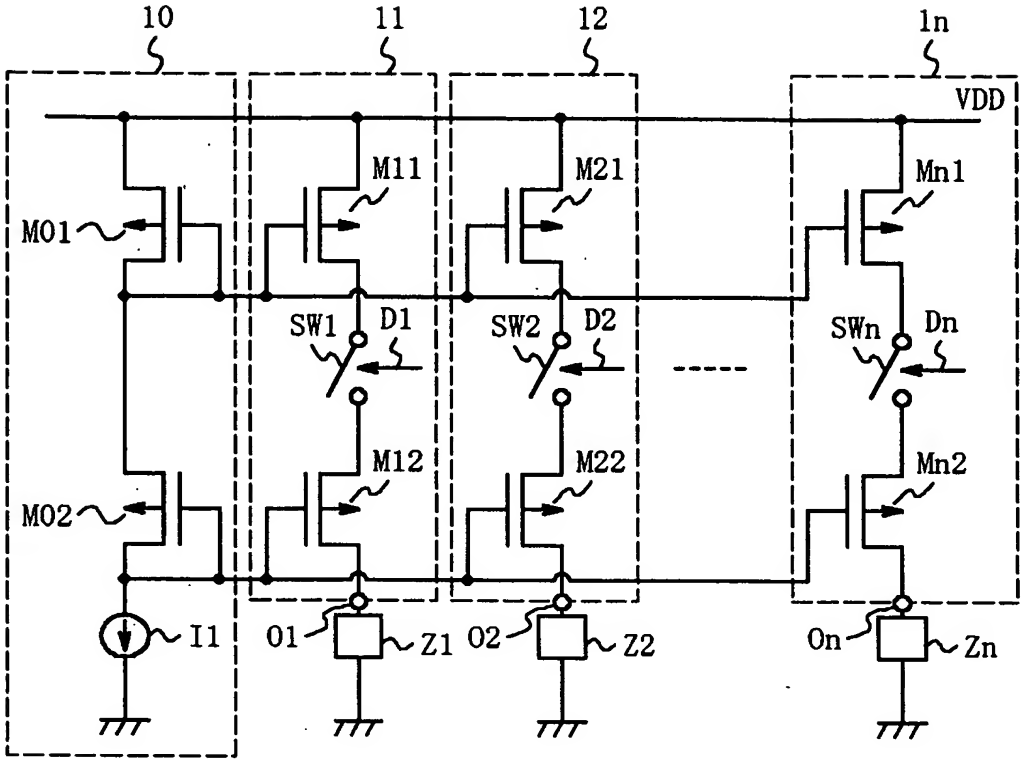

10
11
12
1n
VDD
M01
M11
M21
Mn1
SW1
D1
SW2
D2
SWn
Dn
M12
M22
Mn2
M02
I1
O1
Z1
O2
Z2
On
Zn

Fig. 7

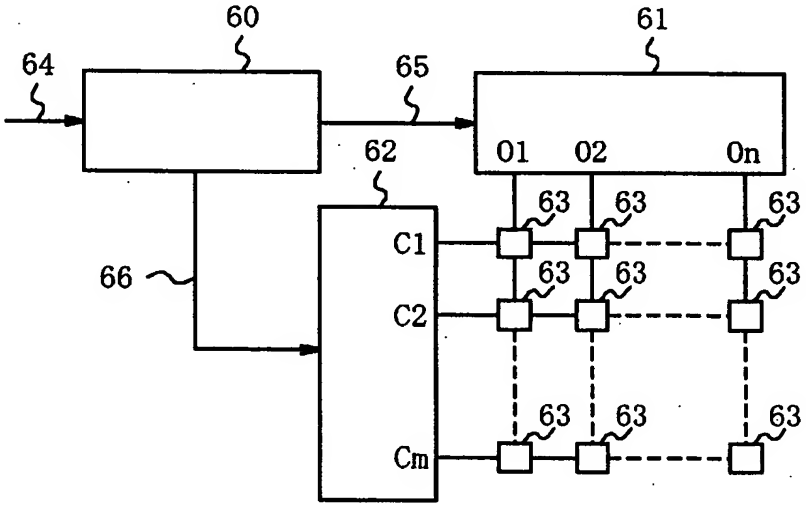
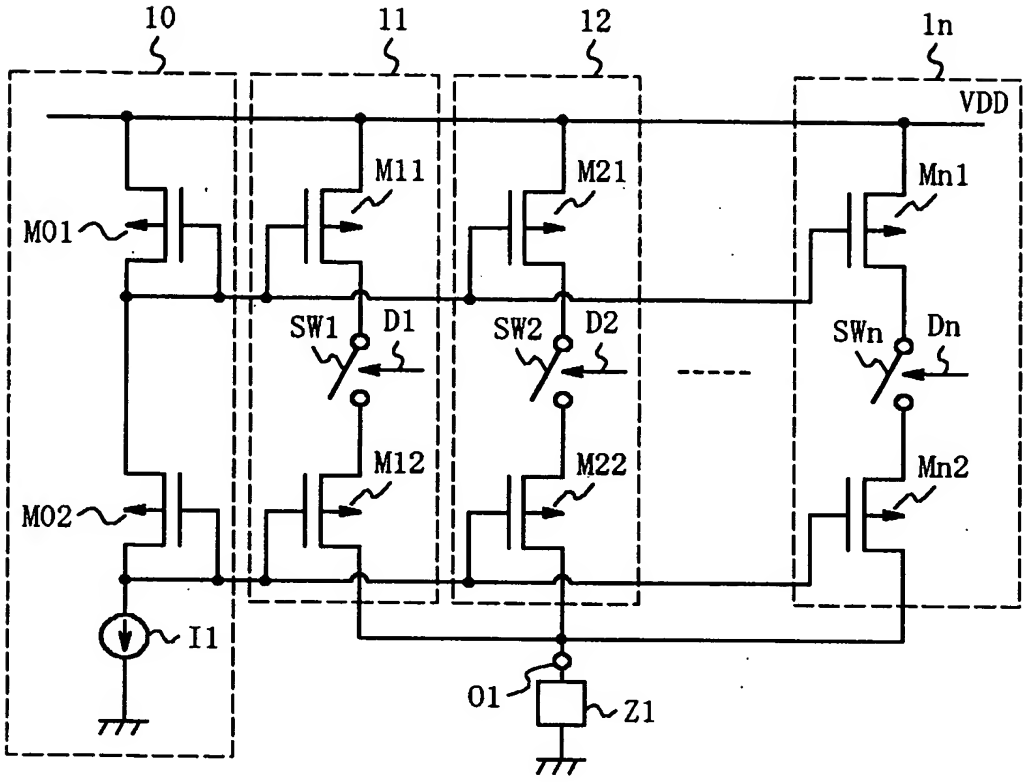

60
61
64
65
62
O1
O2
On
63
C1
C2
Cm
66

Fig. 6


10
11
12
1n
VDD
M01
M11
M21
Mn1
SW1
D1
SW2
D2
SWn
Dn
M02
M12
M22
Mn2
I1
O1
Z1

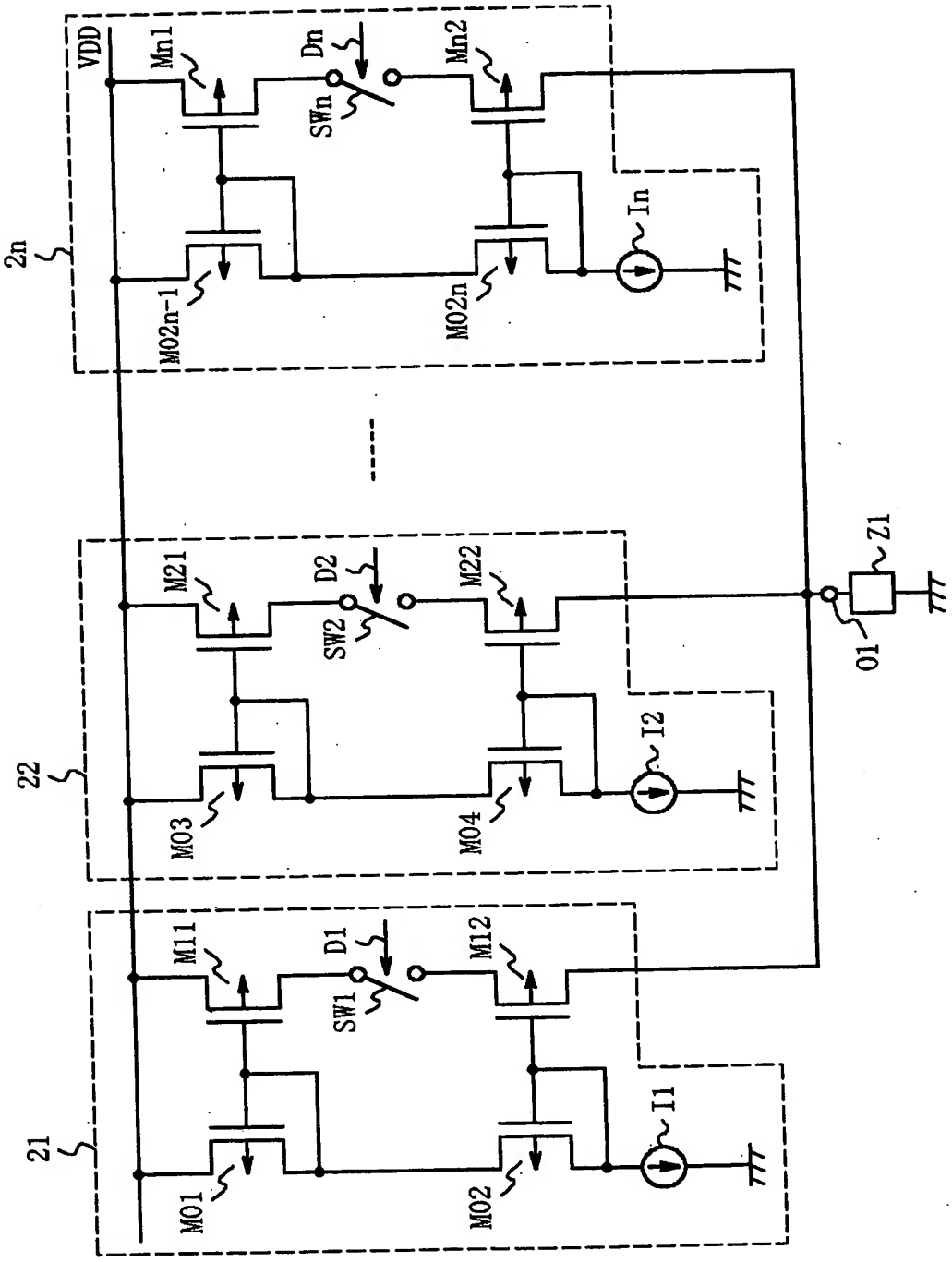

VDD
Mn1
Dn
SWn
Mn2
In
2n
MO2n-1
MO2n
M21
D2
SW2
M22
Z1
O1
I2
22
MO3
MO4
M11
D1
SW1
M12
I1
21
MO1
MO2

Fig. 8

Fig. 9

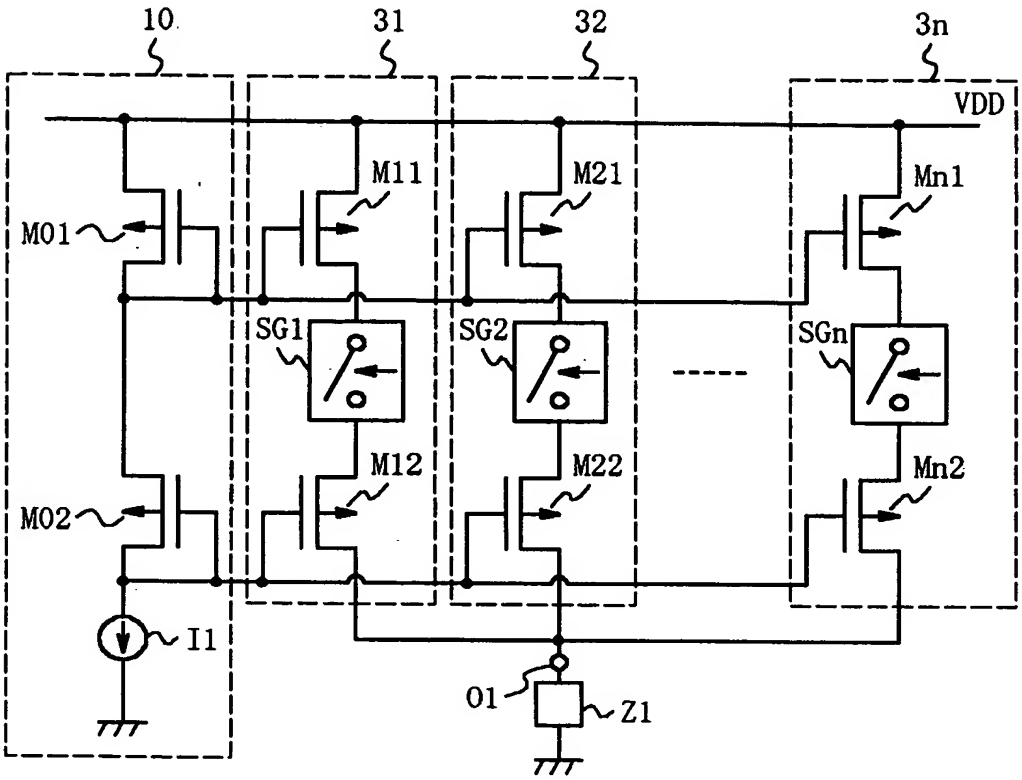

10
31
32
3n
VDD
M01
M11
M21
Mn1
SG1
SG2
SGn
M12
M22
Mn2
M02
I1
O1
Z1

Fig. 10

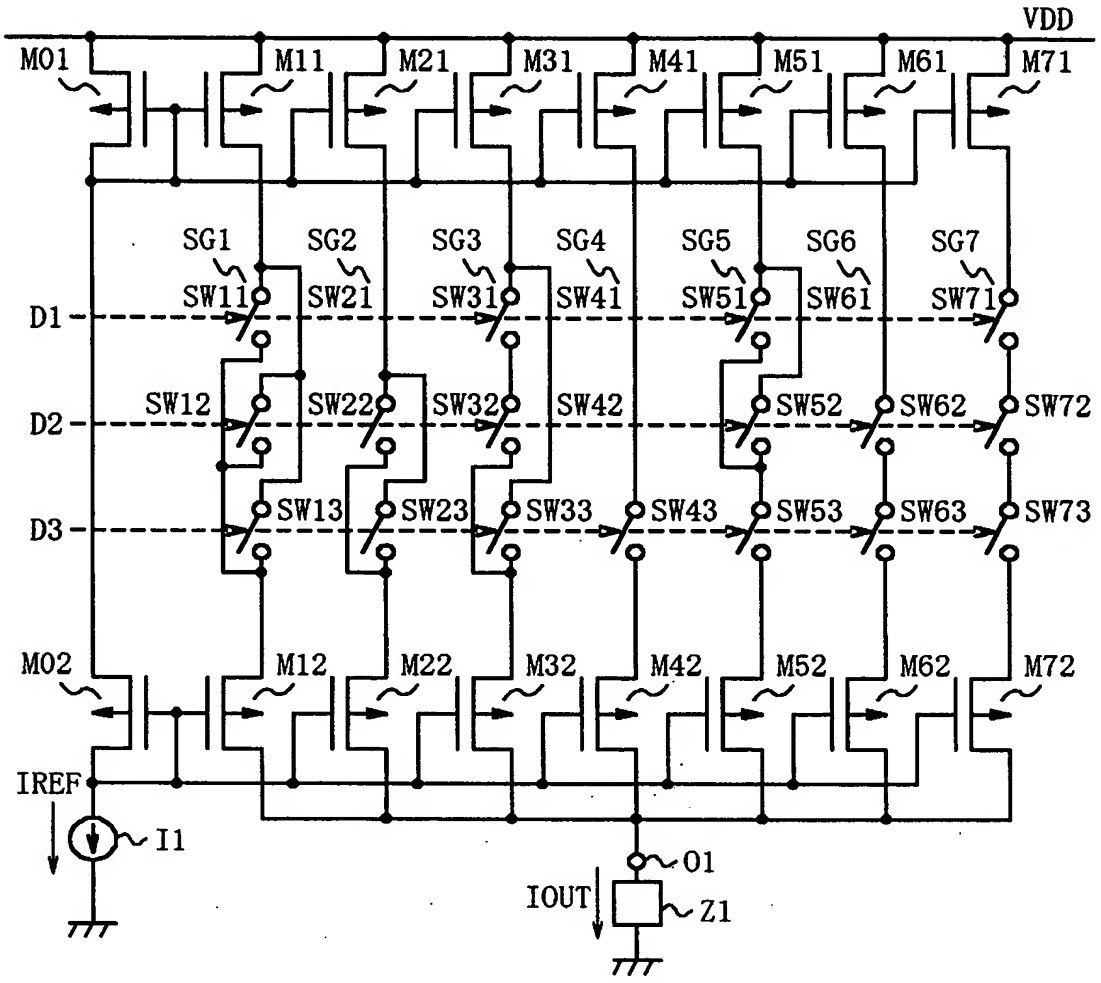


Fig. 11

D3 D2 D1	switch means that are ON	IOUT
0 0 0	no switch means	0
0 0 1	SW11, SW31, SW51, SW71	IREF
0 1 0	SW12, SW22, SW32, SW52, SW62, SW72	2IREF
0 1 1	SW11, SW12, SW22, SW31, SW32, SW51, SW52, SW62, SW71, SW72	3IREF
1 0 0	SW13, SW23, SW33, SW43, SW53, SW63, SW73	4IREF
1 0 1	SW11, SW13, SW23, SW31, SW33, SW43, SW51, SW53, SW63, SW71, SW73	5IREF
1 1 0	SW12, SW13, SW22, SW23, SW32, SW33, SW43, SW52, SW53, SW62, SW63, SW72, SW73	6IREF
1 1 1	SW11, SW12, SW13, SW22, SW23, SW31, SW32, SW33, SW43, SW51, SW52, SW53, SW62, SW63, SW71, SW72, SW73	7IREF